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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,945	07/23/2003	Jerry G. Jex	42P15876	9920

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EXAMINER	
TSE, YOUNG TOI	
ART UNIT	**PAPER NUMBER**
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/625,945	JEX ET AL.	
	Examiner	Art Unit	
	YOUNG T. TSE	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,13-20 and 22-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,13-20 and 22-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. The indicated allowability of claims 2-3, 12-13, 17-18, 21 and 23-28 is withdrawn in view of the newly discovered reference(s) to Scott et al. (U.S. Patent No. 6,137,827) and Simmon et al. (U.S. Publication No. 2001/0006538 A1). Rejections based on the newly cited reference(s) follow.

Drawings

2. The drawings were received on January 22, 2007. These drawings are acceptable.

Specification

The disclosure is objected to because of the following informalities: at page 9, line 29, "Cycle" should be "The complementary cycle". Appropriate correction is required.

Claim Objections

3. Claims 15, 22 and 27 are objected to because of the following informalities:

In claim 15, line 2, "the full cycle encoded signal" should be "the full cycle encoded signal and the complementary cycle encoded signal"; and line 5, "the full cycle encoded signal" should be "the cycle encoded signal".

In claim 22, line 1, "claim 16" should be "claim 17" because without the complementary cycle encoded circuit or signal, the recovered values provided by the receiver can't obtain the inverse of the data input signal.

In claim 27, line 2, "the full cycle encoded signal" should be "the full cycle encoded signal and the complementary cycle encoded signal".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 24 and 28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The terms "a previous data time segment" (see claim 24, line 4) and "no data time segment" (see claim 27, line 2) are vague and indefinite since the precedent claim 23 does not recite a data time segment(s).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 10-11, 14-17, 19-20, 22-23 and 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Scott et al., U.S. Patent No. 6,137,827 (hereinafter "Scott") in view of Pfiffner (U.S. Patent No. 5,623,518).

Scott discloses a block diagram showing a unidirectional isolation system shown in Fig. 2 and a bidirectional isolation system shown in Fig. 7. Each of the isolation systems comprises a transmitter chip 225 and a receiver chip 226. The transmitter chip includes at least an encoder circuit 214/702 for encoding a data signal from an ADC converter 201/701 and a periodic reference signal from an oscillator 202/704 to provide a cycle encoded signal and a differential cycle encoded signal to the receiver chip through a driver 214/703. The receiver chip includes at least a clock recovery circuit 216/707 and a decoder 217/708 for decoding and recovering the cycle or differential cycle encoded signal to the original digital signal. See col. 7, line 50 to col. 8, line 28 and col. 9, line 47 to col. 11, line 28.

With respect to claims 10-11, 16-17, 19, 23, 25 and 28, the encoder circuit 702 generates a cycle encoded signal and a complementary cycle encoded signal to the receiver chip through the driver 703, based on the digital signal and the periodic reference signal generated by the oscillator 704. However, Scott does not explicitly show the detail embodiment of the encoder circuit or teach that the cycle encoded signal is formed of continuously joined portions of encoding signals during successive data time segments, wherein some of the encoding signals have a different frequency than others of the encoding signals and some of the encoding signals have a different phase than others of the encoding signals.

Pfiffner discloses a system in each of Figs. 2A to 2D, wherein each of the systems comprises a transmitter section and a receiver section. In Fig. 2A, the transmitter section comprises a CPU 30, a D/A converter 32, a BPS filter 34 and a TFA transformer 36 and the receiver section comprises a TFE transformer 42, a BPE filter 40, a COMP comparator 38 and the CPU 30. The transmitter section includes a cycle encoding circuit which could be one of or the combination of the CPU 30, the D/A converter 32, the BPS filter 34 and the TFA transformer 36 to receive a data input signal 28 and to provide a full cycle encoded signal 10 as shown in Fig. 1A in response thereto by continuously joining portions of different encoding signals, wherein some of the encoding signals have a different frequency than others of the encoding signals and some of the encoding signals have a different phase than others of the encoding signals, and wherein data is represented in data time segments of the full cycle

encoded signal and no data time segment has more than one cycle of an encoding signal. See column 6, lines 38-52.

Therefore, it would have been obvious to one of ordinary skill in the art to recognize that an encoding circuit is capable of having a different phase than others of the encoding signals, and wherein data is represented in data time segments of the cycle encoded signal and no data time segment has more than one cycle of an encoding signal as taught by Pfiffner in order to processing the cycle encoded signal of the period reference signal.

With respect to claims 14, 20 and 26, as shown in Fig. 1A, wherein the encoding signals shown in the FSK signal 10 include a first signal (first bit) with frequency ft, a second signal (second bit) that is an inverse of the first signal, a third signal (third bit) that has a frequency fn, and a fourth signal (fifth bit) that is an inverse of the third signal.

With respect to claims 15 and 27, the receiver chip includes an initial receiving circuit (262 of Fig. 13B) to receive the cycle encoded signal, a delay circuit (840 of Fig. 11) to delay at least one signal or two signals provided by the initial receiving circuit, and a logic circuit (844 and 846 of Fig. 11) to receive at least one signal or two signals from the delay circuit and in response thereto to provide a data out signal which includes the recovered values of the digital data signal.

With respect to claim 22, it would have been obvious and well known to a person skill in the art to include an inverter circuit in the output of Scott's decoder circuit for inverting the output of the recovered output signal in order to recover the inverse of the encoded input signal.

9. Claims 1-11, 13-20 and 22-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Simon et al., U.S. Publication No. 2001/0006538 A1 (hereinafter "Simon") in view of Pfiffner (U.S. Patent No. 5,623,518).

Scott discloses a block diagram showing a transceiver chip in Fig. 5A and 5B comprising a transmitter chip 540, a receiver chip 530, a calibration circuit 520 and a clock synchronization circuit 560. Fig. 6 shows the detail transceiver chip 510 of the transmitter chip 540 and the receiver chip 530. Fig. 7A shows the detail embodiment of the transmitter chip, which includes a phase modulation circuit 640, a width modulation circuit 630, an amplitude modulation circuit 620 and a strobe transmitter 790. Fig. 9A shows the detail embodiment of the receiver chip, which includes differential to single-ended amplifiers 920(a) and 920(b), a unit AND gate 930, a unit OR gate 940(a), an amplitude demodulation circuit 660, a phase demodulation circuit 670, a width demodulation circuit 680, a set of latches 970(a)- 970(d) a strobe receiver 902. See paragraphs [[0076] to [0090] and [0097] to [0105].

With respect to claims 1-4, 10-11, 13, 16-19, 23-25 and 28, the transmitter chip 540 shown in Fig. 7A comprises an encoder circuit and a complementary encoder circuit (640, 630, 620) including a multiplexer circuit 720 generates a cycle encoded signal and a complementary cycle encoded signal to the receiver chip 530, based on the digital signals (1 phase bit, two width bits, 1 amplitude bit) and a periodic reference signal generated by the clock synchronization circuit 560. The multiplexer selects one of the delay signals (722, 724, 726, 728) based on the control of the width bits. However, Scott does not explicitly show the detail embodiment of the encoder circuit(s)

or teach that the cycle encoded signal is formed of continuously joined portions of encoding signals during successive data time segments, wherein some of the encoding signals have a different frequency than others of the encoding signals and some of the encoding signals have a different phase than others of the encoding signals.

Pfiffner discloses a system in each of Figs. 2A to 2D, wherein each of the systems comprises a transmitter section and a receiver section. In Fig. 2A, the transmitter section comprises a CPU 30, a D/A converter 32, a BPS filter 34 and a TFA transformer 36 and the receiver section comprises a TFE transformer 42, a BPE filter 40, a COMP comparator 38 and the CPU 30. The transmitter section includes a cycle encoding circuit which could be one of or the combination of the CPU 30, the D/A converter 32, the BPS filter 34 and the TFA transformer 36 to receive a data input signal 28 and to provide a full cycle encoded signal 10 as shown in Fig. 1A in response thereto by continuously joining portions of different encoding signals, wherein some of the encoding signals have a different frequency than others of the encoding signals and some of the encoding signals have a different phase than others of the encoding signals, and wherein data is represented in data time segments of the full cycle encoded signal and no data time segment has more than one cycle of an encoding signal. See column 6, lines 38-52.

Therefore, it would have been obvious to one of ordinary skill in the art to recognize that an encoding circuit is capable of having a different phase than others of the encoding signals, and wherein data is represented in data time segments of the cycle encoded signal and no data time segment has more than one cycle of an

encoding signal as taught by Pfiffner in order to processing the cycle encoded signal of the period reference signal.

With respect to claims 5 and 6 as shown in Fig. 1A, clearly, the periodic reference signal has period that is equal to the time length of the data time segments and has a period that is equal to the time length of a data bit cell of the data input signal.

With respect to claims 7, 14, 20 and 26, as shown in Fig. 1A, wherein the encoding signals shown in the FSK signal 10 include a first signal (first bit) with frequency ft, a second signal (second bit) that is an inverse of the first signal, a third signal (third bit) that has a frequency fn, and a fourth signal (fifth bit) that is an inverse of the third signal.

With respect to claim 8, wherein the full cycle encoded signal represents a 0 or a 1 depending on the value of the data.

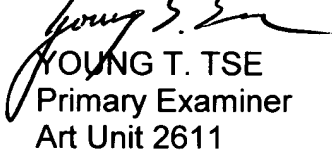
With respect to claims 9, 15 and 27, the receiver chip includes an initial receiving circuit (920(a) and 920(b)) to receive the cycle encoded signal, a delay circuit (930 and 940(a)) to delay at least one signal or two signals provided by the initial receiving circuit, and a logic circuit (970(a) to 970(d)) to receive at least one signal or two signals from the delay circuit and in response thereto to provide a data out signal which includes the recovered values of the digital data signal.

With respect to claim 22, it would have been obvious and well known to a person skill in the art to include an inverter circuit in the output of Scott's decoder circuit for inverting the output of the recovered output signal in order to recover the inverse of the encoded input signal.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOUNG T. TSE whose telephone number is (571) 272-3051. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



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Art Unit 2611